Abstract

An apparatus and method for efficiently generating a zero value may be used with instruction set architectures which do not support an explicit zero reading register (r0) to speed execution. The present invention includes a physical register that reads out a value

5   of zero when accessed, and a Zero Instruction Logic (ZIL) unit that identifies instructions that appear to be compensating for the lack of an r0 register, and modify the stream of instructions to utilize the physical register. Embodiments of the present invention may decrease the number of instructions that must be executed, and may decrease false dependencies between instructions allowing more scheduling flexibility.